## IN THE UNITED STATES PATENT AND TRADEMAKK OFFICE

Group Art Unit: 2829

Examiner: Jermele M. Hollington

) INFORMATION DISCLOSURE **STATEMENT** 

Re PATENT APPLICATION Of:

Applicant(s) : Mikio OHTAKI

Serial No. : 09/904,663

Filed : July 16, 2001

For : SEMICONDUCTOR DEVICE

TEST METHOD

Attorney Ref.: KAN 120 D1

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

This is an information disclosure statement submitted in compliance with the timing requirements of 37 C.F.R. §1.97(c), i.e., after a first Office Action on the merits but before Final Rejection and/or Notice of Allowance. Pursuant to 37 C.F.R. § 1.97(e)(1), it is certified that each item submitted with this Information Disclosure Statement was first cited in an Office Action from the Japanese Patent Office in a counterpart foreign application on June 24, 2003, that is, less than three months prior to filing this Information Disclosure Statement.

Attached are a copy of a Japanese Office Action and three Japanese Patents with English The relevance of the publications can be gleaned from the attached English language Abstracts. The documents are listed on the attached Form PTO-1449.

Consideration of the submitted documents is respectfully requested.

Respectfully submitted,

August 20, 2003

Phillip G. Avruch - Reg. No. 46,076

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INFORMATION DISCLOSURE STATEMENT				Applicant Mikio OHTAKI				
				Filing Date July 16, 2001	Group 282	Group 2829		
				U.S. PATENT DOCUMENTS				
Examiner Initial		Document Number	Date	Name	Class	Sub- Class	Filing Date	
	AA							
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		Document Number	Date	Country	Class	Sub- Class	Trans lation	
	Al	10-189670	7/21/98	JAPAN			Abstract	
	AJ	11-17076	1/22/99	JAPAN			Abstract	
	AK	64-001252	1/5/89	JAPAN			Abstract	
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